EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Aly Dossa (Reg. No. 63,372) on 6/17/09.

The claims and the Specification have been amended in the Examiner's Amendment.

Please amend the originally-filed specification as follows:

Please replace paragraphs [0064]-[0066] with the following paragraphs:

-- The term "computer-readable medium" as used herein refers to any medium that participates in providing instructions to processing unit 904 for execution. Such a medium may take many forms, comprising ~~but not limited to,~~ non-volatile media [[,]] and/or volatile media~~, and transmission media~~. Non-volatile media comprises, for example, optical or magnetic disks, such as storage device 910. Volatile media comprises dynamic memory, such as main memory 906. ~~Transmission media comprises coaxial cables, copper wire, and fiber optics, comprising the wires that comprise bus 902. Transmission media can also take the form of acoustic or electromagnetic waves, such as those generated during radio-wave, infra-red, and optical data communications.~~

Common forms of computer-readable media comprise, for example, a floppy disk, a flexible disk, a hard disk, a magnetic tape, or any other magnetic medium, a CD-ROM, any other optical medium, punch cards, paper tape, any other physical medium with patterns of holes, a RAM, a

PROM, and EPROM, a FLASH-EPROM, any other memory chip or cartridge, ~~a carrier wave as described hereinafter,~~ or any other storage medium from which a computer can read.

Various forms of computer readable media may be involved in carrying one or more sequences of one or more instructions to processing unit 904 for execution. For example, the instructions may initially be carried on a magnetic disk of a remote computer. The remote computer can load the instructions into its dynamic memory and send the instructions to computer system 900. ~~over a telephone line using a modem. A modem local to computer system 900 can receive the data on the telephone line and use an infra-red transmitter to convert the data to an infra-red signal. An infra-red detector can receive the data carried in the infra-red signal and appropriate circuitry can place the data on bus 902.~~ Bus 902 of computer system 900 carries the data to main memory 906, from which processing unit 904 retrieves and executes the instructions. The instructions received by main memory 906 may optionally be stored on storage device 910 either before or after execution by processing unit 904.--

The claims in the application have been amended as follows:

1. – 25. (Canceled)

26. (Currently Amended) A method performed by an operating system executing within a computer system having different types of physical processing modules, the method comprising:

receiving a first set of parametric information pertaining to a first physical processing module (PPM), the first PPM having a first architecture;

~~receiving a second set of parametric information pertaining to a second PPM, the second PPM having a second architecture, wherein the first architecture is different from the second architecture;~~

constructing a first abstraction of the first PPM based, at least partially, upon the first set of parametric information, the first abstraction comprising an indication of how many logical processing entities are provided by the first PPM, the first abstraction further comprising operational information indicating one or more operational characteristics of the first PPM;

determining that a second abstraction for a second PPM does not exist, the second PPM having a second architecture, wherein the first architecture is different from the second architecture;

receiving a second set of parametric information pertaining to the second PPM;

constructing [[a]] the second abstraction of the second PPM based, at least partially, upon the second set of parametric information, the second abstraction comprising an indication of how many logical processing entities are provided by the second PPM, the second abstraction further comprising operational information indicating one or more operational characteristics of the second PPM, wherein the second abstraction is different from the first abstraction to reflect at least one difference between the first architecture of the first PPM and the second architecture of the second PPM; and

dispatching ~~determining~~, based on the at least one difference between the first architecture of the first PPM and the second architecture of the second PPM and ~~one selected from a group consisting of~~ the operational information in the first abstraction ~~and the operational information in the second abstraction, whether to dispatch~~ an execution thread for execution to ~~one selected from a group consisting of~~ one of the logical processing entities of the first PPM ~~and one of the logical processing entities of the second PPM; wherein the second abstraction is different from the first abstraction to reflect the differences between the first architecture of the first PPM and the second architecture of the second PPM~~.

27. (Currently Amended) The method of claim 26, wherein the first PPM comprises a first physical processing core which supports a single hardware thread, wherein the second PPM

comprises a second physical processing core which supports a plurality of hardware threads, wherein constructing ~~constructing~~ the first abstraction comprises indicating the first physical processing core as a single logical processing entity, and wherein constructing the second abstraction comprises indicating the second physical processing core as a plurality of logical processing entities.

28. (Original) The method of claim 27, wherein constructing the second abstraction comprises indicating that the plurality of logical processing entities corresponding to the second physical processing core share one or more resources of the second PPM.

29. – 53. (Canceled)

54. (Currently Amended) A computer readable ~~storage~~ medium carrying instructions for an operating system, wherein the instructions, when executed in a computer system ~~having different types of physical processing modules~~, cause the computer system to perform the operations of:

receiving a first set of parametric information pertaining to a first physical processing module (PPM), the first PPM having a first architecture;

~~receiving a second set of parametric information pertaining to a second PPM, the second PPM having a second architecture, wherein the first architecture is different from the second architecture;~~

constructing a first abstraction of the first PPM based, at least partially, upon the first set of parametric information, the first abstraction comprising an indication of how many logical processing entities are provided by the first PPM, the first abstraction further comprising operational information indicating one or more operational characteristics of the first PPM;

determining that a second abstraction for a second PPM does not exist, the second PPM having a second architecture, wherein the first architecture is different from the second architecture;

receiving a second set of parametric information pertaining to the second PPM;

constructing a second abstraction of the second PPM based, at least partially, upon the second set of parametric information, the second abstraction comprising an indication of how many logical processing entities are provided by the second PPM, the second abstraction further comprising operational information indicating one or more operational characteristics of the second PPM, wherein the second abstraction is different from the first abstraction to reflect at least one difference between the first architecture of the first PPM and the second architecture of the second PPM; and

dispatching ~~determining~~, based on the at least one difference between the first architecture of the first PPM and the second architecture of the second PPM and ~~selected from a group consisting of~~ the operational information in the first abstraction ~~and the operational information in the second abstraction, whether to dispatch~~ an execution thread for execution to ~~one selected from a group consisting of~~ one of the logical processing entities of the first PPM ~~and one of the logical processing entities of the second PPM~~;

~~wherein the second abstraction is different from the first abstraction to reflect the differences between the first architecture of the first PPM and the second architecture of the second PPM~~.

55. (Previously Presented) The computer readable ~~storage~~ medium of claim 54, wherein the first PPM comprises a first physical processing core which supports a single hardware thread, wherein the second PPM comprises a second physical processing core which supports a plurality of hardware threads, wherein constructing the first abstraction comprises indicating the first physical processing core as a single logical processing entity, and wherein constructing the second abstraction comprises indicating the second physical processing core as a plurality of logical processing entities.

56. (Previously Presented) The computer readable ~~storage~~ medium of claim 55, wherein constructing the second abstraction comprises indicating that the plurality of logical

processing entities corresponding to the second physical processing core share one or more resources of the second PPM.

57. – 81. (Canceled)

82. (Previously Presented) A computer system comprising:

a first physical processing module (PPM) having a first architecture;

~~a second PPM having a second architecture, wherein the first architecture is different from the second architecture; and~~

an operating system executing within the computer system, wherein the operating system performs the operations of:

receiving a first set of parametric information pertaining to the first PPM;

~~receiving a second set of parametric information pertaining to the second PPM,;~~

constructing a first abstraction of the first PPM based, at least partially, upon the first set of parametric information, the first abstraction comprising an indication of how many logical processing entities are provided by the first PPM, the first abstraction further comprising operational information indicating one or more operational characteristics of the first PPM;

determining that a second abstraction for a second PPM does not exist, the second PPM having a second architecture, wherein the first architecture is different from the second architecture;

receiving a second set of parametric information pertaining to the second PPM;

constructing a second abstraction of the second PPM based, at least partially, upon the second set of parametric information, the second abstraction comprising an indication of how many logical processing entities are provided by the second PPM, the second abstraction further comprising operational information indicating one or more operational characteristics of the second PPM, wherein the second abstraction is different from the first abstraction to reflect the differences between the first architecture of the first PPM and the second architecture of the second PPM; and

dispatching ~~determining~~, based on the at least one difference between the first architecture of the first PPM and the second architecture of the second PPM and ~~selected from a group consisting of~~ the operational information in the first abstraction ~~and the operational information in the second abstraction~~, ~~whether to dispatch~~ an execution thread for execution to ~~one selected from a group consisting of~~ one of the logical processing entities of the first PPM ~~and one of the logical processing entities of the second PPM~~;

~~wherein the second abstraction is different from the first abstraction to reflect the differences between the first architecture of the first PPM and the second architecture of the second PPM~~.

83. (Previously Presented) The computer system of claim 82, wherein the first PPM comprises a first physical processing core which supports a single hardware thread, wherein the second PPM comprises a second physical processing core which supports a plurality of hardware threads, wherein constructing the first abstraction comprises indicating the first physical processing core as a single logical processing entity, and wherein constructing the second abstraction comprises indicating the second physical processing core as a plurality of logical processing entities.

84. (Previously Presented) The computer system of claim 83, wherein constructing the second abstraction comprises indicating that the plurality of logical processing entities corresponding to the second physical processing core share one or more resources of the second PPM.

85. (Previously Presented) The method of claim 26,

wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and

wherein the second PPM has a single processing core capable of supporting an m number of hardware threads, where m is an integer greater than one.

86. (Previously Presented) The method of claim 85, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an m number of logical processing entities.

87. (Previously Presented) The method of claim 86, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the m logical processing entities of the second PPM.

88. (Previously Presented) The method of claim 87, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that the m logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

89. (Previously Presented) The method of claim 26,

wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supporting a p number of hardware threads, where p is an integer greater than one.

90. (Previously Presented) The method of claim 89, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

91. (Previously Presented) The method of claim 90, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources

shared by then logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

92. (Previously Presented) The method of claim 91, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

93. (Previously Presented) The method of claim 26,

wherein the first PPM has a single processing core capable of supporting an n number of hardware threads, where n is an integer greater than one; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supporting a p number of hardware threads, where p is an integer greater than one.

94. (Previously Presented) The method of claim 93, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

95. (Previously Presented) The method of claim 94, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

96. (Previously Presented) The method of claim 95, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share one

or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

97. (Previously Presented) The method of claim 26, further comprising:

accessing the first abstraction and/or the second abstraction.

98. (Previously Presented) The method of claim 97, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the second PPM.

99. (Previously Presented) The method of claim 98, wherein determining whether to dispatch an execution thread comprises:

determining, based at least partially upon the resource sharing information in the first abstraction and/or the resource sharing information in the second abstraction, whether to dispatch an execution thread to one of the logical processing entities of the first PPM or one of the logical processing entities of the second PPM to be executed thereby.

100. (Previously Presented) The method of claim 99, wherein the resource sharing information in the first abstraction indicates that the logical processing entities of the first PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

101. (Previously Presented) The method of claim 100, wherein the resource sharing information in the second abstraction indicates that the logical processing entities of the second PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

102. (Previously Presented) The computer readable ~~storage~~ medium of claim 54, wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and wherein the second PPM has a single processing core capable of supporting an m number of hardware threads, where m is an integer greater than one.

103. (Previously Presented) The computer readable ~~storage~~ medium of claim 102, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an m number of logical processing entities.

104. (Previously Presented) The computer readable ~~storage~~ medium of claim 103, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the m logical processing entities of the second PPM.

105. (Previously Presented) The computer readable ~~storage~~ medium of claim 104, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that the m logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

106. (Previously Presented) The computer readable ~~storage~~ medium of claim 54,

wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supporting a p number of hardware threads, where p is an integer greater than one.

107. (Previously Presented) The computer readable ~~storage~~ medium of claim 106, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

108. (Previously Presented) The computer readable ~~storage~~ medium of claim 107, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

109. (Previously Presented) The computer readable ~~storage~~ medium of claim 108, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

110. (Previously Presented) The computer readable ~~storage~~ medium of claim 54,

wherein the first PPM has a single processing core capable of supporting an n number of hardware threads, where n is an integer greater than one; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supposing a p number of hardware threads, where p is an integer greater than one.

111. (Previously Presented) The computer readable ~~storage~~ medium of claim 1 10, wherein the first abstraction indicates that the first PPM provides an n number of logical processing

entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

112. (Previously Presented) The computer readable ~~storage~~ medium of claim 11 1, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

113. (Previously Presented) The computer readable ~~storage~~ medium of claim 112, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

114. (Previously Presented) The computer readable ~~storage~~ medium of claim 54, wherein the instructions cause the computer system to further perform the operations of:

accessing the first abstraction and/or the second abstraction.

115. (Previously Presented) The computer readable ~~storage~~ medium of claim 114, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the second PPM.

116. (Previously Presented) The computer readable ~~storage~~ medium of claim 115, wherein determining whether to dispatch an execution thread comprises:

determining, based at least partially upon the resource sharing information in the first abstraction and/or the resource sharing information in the second abstraction, whether to dispatch an execution thread to one of the logical processing entities of the first PPM or one of the logical processing entities of the second PPM to be executed thereby.

117. (Previously Presented) The computer readable ~~storage~~ medium of claim 116, wherein the resource sharing information in the first abstraction indicates that the logical processing entities of the first PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

118. (Previously Presented) The computer readable ~~storage~~ medium of claim 117, wherein the resource sharing information in the second abstraction indicates that the logical processing entities of the second PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

119. (Previously Presented) The computer system of claim 82,

wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and

wherein the second PPM has a single processing core capable of supporting an m number of hardware threads, where m is an integer greater than one.

120. (Previously Presented) The computer system of claim 119, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an m number of logical processing entities.

121. (Previously Presented) The computer system of claim 120, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information

indicating one or more resources shared by the m logical processing entities of the second PPM.

122. (Previously Presented) The computer system of claim 121, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that the m logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

123. (Previously Presented) The computer system of claim 82,

wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supporting a p number of hardware threads, where p is an integer greater than one.

124. (Previously Presented) The computer system of claim 123, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

125. (Previously Presented) The computer system of claim 124, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

126. (Previously Presented) The computer system of claim 125, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction

indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

127. (Previously Presented) The computer system of claim 82,

wherein the first PPM has a single processing core capable of supporting an n number of hardware threads, where n is an integer greater than one; and

wherein the second PPM has an m number of processing cores, wherein m is an integer greater than one, each of the m processing cores capable of supporting a p number of hardware threads, where p is an integer greater than one.

128. (Previously Presented) The computer system of claim 127, wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

129. (Previously Presented) The computer system of claim 128, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

130. (Previously Presented) The computer system of claim 129, wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

131. (Previously Presented) The computer system of claim 82, wherein the operating system further performs the operations of:

accessing the first abstraction and/or the second abstraction.

132. (Previously Presented) The computer system of claim 131, wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the second PPM.

133. (Previously Presented) The computer system of claim 132, wherein determining whether to dispatch an execution thread comprises:

determining, based at least partially upon the resource sharing information in the first abstraction and/or the resource sharing information in the second abstraction, whether to dispatch an execution thread to one of the logical processing entities of the first PPM or one of the logical processing entities of the second PPM to be executed thereby.

134. (Previously Presented) The computer system of claim 133, wherein the resource sharing information in the first abstraction indicates that the logical processing entities of the first PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

135. (Previously Presented) The computer system of claim 134, wherein the resource sharing information in the second abstraction indicates that the logical processing entities of the second PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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